IN THE CLAIMS:

1. (Original) A method for manufacturing a semiconductor memory device comprising the steps of:

forming a first insulating layer on a semiconductor substrate;

forming a plurality of bit lines on the first insulating layer;

forming an oxidation preventing layer over substantially the entire surface of the bit lines and the first insulating layer;

forming a second insulating layer on the oxidation preventing layer;

forming a contact hole exposing a portion of the semiconductor substrate by patterning the second insulating layer, the oxidation preventing layer, and the first insulating layer;

forming a storage electrode over the second insulating layer and connected to the portion of the semiconductor substrate through the contact hole; and

sequentially forming a dielectric layer and a plate electrode on the storage electrode.

2. (Original) The method of claim 1, wherein the oxidation preventing layer comprises a nitride layer.

3. (Original) The method of claim 2, wherein the nitride layer is formed to a thickness equal to or less than about 1,000 angstroms.

4. (Original) The method of claim 1, wherein each of the bit lines has sidewalls and a top, and wherein the oxidation preventing layer is formed to be thicker on the sidewalls and on the top of the bit lines than on the first insulating layer.

5. (Original) The method of claim 2, wherein the nitride layer is formed by a low pressure chemical vapor deposition (LPCVD) process.

6. (Original) The method of claim 5, wherein the LPCVD process is performed at a temperature of about 800~1000° C under a pressure of about 1 torr or less using a gas mixture of dichlorosilane (SiH_2C1_2) and ammonia (NH_3) as a reactant gas.

7. (Original) The method of claim 2, wherein the nitride layer is formed by a rapid thermal nitridation (RTN) process.

8. (Original) The method of claim 7, wherein the RTN process is performed at a temperature of about 800~1000° C under a pressure of atmospheric pressure or less using an ammonia (NH_3) gas as a reactant gas.

9. (Original) The method of claim 1, wherein the step of forming the oxidation preventing layer is performed by nitriding the surface of the bit lines and the first insulating layer.

10. (Original) The method of claim 9, wherein the nitriding step is performed by a plasma process using an ammonia (NH_3) gas.

11. (Original) The method of claim 10, wherein the plasma process is performed at a temperature of about 200~400° C for more than about one minute.

12. (Original) The method of claim 9, wherein the nitriding step is performed by a thermal annealing process.

13. (Original) The method of claim 12, wherein the thermal annealing process is performed at a temperature of about 800~900° C for more than about thirty minutes.

14. (Original) The method of claim 9, wherein the nitriding step is performed by a rapid thermal process.

15. (Original) The method of claim 14, wherein the rapid thermal process is performed at a temperature of about 800~1000° C for more than about one minute.

16. (Original) The method of claim 1, wherein the contact hole has a sidewall, and wherein the step of forming a storage electrode is preceded by a step of forming a spacer on the sidewall of the contact hole.

17. (Original) The method of claim 1, wherein the first and second insulating layers comprise a borophosphosilicate glass (BPSG) or an undoped silicate glass (USG).

18. (Original) The method of claim 1, wherein a nitride layer and an oxide layer are sequentially formed on the second insulating layer prior to the step of forming the contact hole.

19. (Original) A method for manufacturing a semiconductor memory device comprising the steps of:

forming a first insulating layer on a semiconductor substrate;

forming a plurality of bit lines on the first insulating layer;

forming a second insulating layer on the bit lines and the first insulating layer;

forming a contact hole exposing a portion of the semiconductor substrate by patterning the second and first insulating layers, wherein the contact hole has a sidewall;

forming a dual spacer by forming a nitride spacer layer on the sidewall of the contact hole, and then forming an oxide spacer layer on the nitride spacer layer;

forming a storage electrode over the second insulating layer and connected to the portion of the semiconductor substrate through the contact hole; and

sequentially forming a dielectric layer and a plate electrode on the storage electrode.

20. (Original) The method of claim 19, wherein the nitride spacer layer and the oxide spacer layer in the dual spacer are each formed to a thickness of about 100~300 angstroms.

21. (Original) The method of claim 20, wherein the oxide spacer layer for the dual spacer is formed of a high temperature oxide (HTO) layer or an undoped silicate glass (USG) layer.

22. (Original) The method of claim 19, wherein the first and second insulating layers comprise a borophosphosilicate glass (BPSG) or an undoped silicate glass (USG).

23. (Original) The method of claim 19, wherein a nitride layer and an oxide layer are sequentially formed on the second insulating layer prior to the step of forming the contact hole.

24. (Original) A method for manufacturing a semiconductor memory device comprising the steps of:

forming a first insulating layer on a semiconductor substrate;

forming a plurality of bit lines on the first insulating layer;

forming a second insulating layer on the bit lines and the first insulating layer;

forming a contact hole exposing the a portion of the semiconductor substrate by patterning the second and the first insulating layers;

forming a storage electrode over the second insulating layer and connected to the portion of the semiconductor substrate through the contact hole;

forming an oxidation preventing layer on the storage electrode; and

sequentially forming a dielectric layer and a plate electrode on the oxidation preventing layer.

25. (Original) The method of claim 24, wherein the step of forming the oxidation preventing layer is performed by nitriding the surface of the storage electrode and an adjacent substrate surface prior to the step of forming the dielectric layer and the plate electrode.

26. (Original) The method of claim 25, wherein the nitriding step is performed by a plasma process using an ammonia (NH_3) gas.

27. (Original) The method of claim 26, wherein the plasma process is performed at about 400° C for about four minutes.

28. (Original) The method of claim 25, wherein the nitriding step is performed by a thermal annealing process.

29. (Original) The method of claim 28, wherein the thermal annealing process is performed at about 800~900° C for about sixty minutes.

30. (Original) The method of claim 25, wherein the nitriding step is performed by a rapid thermal nitridation process.

31. (Original) The method of claim 30, wherein the rapid thermal nitridation process is performed at about 800~1000° C for about ninety seconds.

32. (Original) The method of claim 25, wherein the contact hole has a sidewall, and wherein the step of forming a storage electrode is preceded by a step of forming a spacer on the sidewall of the contact hole.

33. (Original) The method of claim 32, wherein the nitriding step is preceded by a step of surface processing to increase the thickness of the oxidation preventing layer subsequently formed on an exposed portion of the second insulating layer.

34. (Original) The method of claim 24, wherein the first and second insulating layers comprise a borophosphosilicate glass (BPSG) or an undoped silicate glass (USG).

35. (Original) The method of claim 24, wherein a nitride layer and an oxide layer are sequentially formed on the second insulating layer prior to the step of forming the contact hole.

36. (Original) A semiconductor memory device comprising:

a first insulating layer formed on a semiconductor substrate;

bit lines formed on the first insulating layer and connected to a first active region of the semiconductor substrate, the bit lines having a side wall and a top;

an oxidation preventing layer formed on the first insulating layer and on the bit lines, wherein the oxidation preventing layer is thicker on the side walls and on the top of the bit lines than on the first insulating layer;

a second insulating layer covering the oxidation preventing layer;

a storage electrode formed over the second insulating layer and connected to a second active region of the semiconductor substrate through a contact hole formed through the second insulating layer, oxidation preventing layer and first insulating layer, wherein the contact hole has a sidewall;

a dielectric layer covering the storage electrode; and

a plate electrode covering the dielectric layer.

37. (Original) The semiconductor memory device of claim 36, wherein each of the bit lines is comprised of a polysilicon layer and a silicide layer.

38. (Original) The semiconductor memory device of claim 36, wherein the oxidation preventing layer is comprised of a nitride layer.

39. (Original) The semiconductor memory device of claim 38, wherein the thickness of the oxidation preventing layer is less than 1,000 angstroms.

40. (Original) The semiconductor memory device of claim 36, wherein the first insulating layer is comprised of a borophosphosilicate glass (BPSG).

41. (Original) The semiconductor memory device of claim 36, further comprising a spacer formed on the sidewall of the contact hole.

42. (Original) The semiconductor memory device of claim 36, wherein the dielectric layer is comprised of a nitride layer and an oxide layer.

43. (Original) The semiconductor memory device of claim 36, further comprising a first and a second spacer sequentially formed on the sidewall of the contact hole.

Please add the following new claims.

- -44. (New) A method of manufacturing a semiconductor device comprising:

forming a first insulating layer on a semiconductor substrate;

forming a plurality of bit lines on the first insulating layer;

forming an oxidation preventing layer;

forming a second insulating layer;

forming a contact hole exposing a portion of the semiconductor substrate;

forming a storage electrode connected to the portion of the semiconductor substrate through the contact hole;

forming a dielectric layer; and

forming a plate electrode.

45. (New) The method of claim 44, wherein the oxidation preventing layer is formed over substantially the entire surface of the bit lines and the first insulating layer.

46. (New) The method of claim 45, wherein the oxidation preventing layer is a nitride layer.

47. (New) The method of claim 45, wherein the oxidation preventing layer is formed by nitriding the surface of the bit lines and the first insulating layer.

48. (New) The method of claim 47, wherein the nitriding is performed by a process selected from the group consisting of a plasma process using ammonia gas, a thermal annealing process and a rapid thermal process.

49. (New) The method of claim 45, wherein each of the bit lines has sidewalls and a top, and wherein the oxidation preventing layer is formed to be thicker on the sidewalls and on the top of the bit lines than on the first insulating layer.

50. (New) The method of claim 44, wherein the oxidation preventing layer is formed on the storage electrode.

51. (New) The method of claim 50, wherein the oxidation preventing layer is formed by nitriding the surface of the storage electrode and an adjacent substrate surface prior to forming the dielectric layer and the plate electrode.

52. (New) The method of claim 51, wherein the nitriding is performed by a plasma process using an ammonia gas.

53. (New) The method of claim 44, wherein the oxidation preventing layer is a dual spacer.

54. (New) The method of claim 53, wherein the dual spacer is formed by forming a nitride spacer layer on the sidewall of the contact hole and forming an oxide spacer layer on the nitride spacer layer.

55. (New) The method of claim 54, wherein the nitride spacer layer and oxide spacer layer in the dual spacer are each formed to a thickness of from about 100 to 300 angstroms.- -